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METHOD FOR FORMING A REDUCED ACTIVE AREA IN A PHASE CHANGE
MEMORY STRUCTURE

FIELD OF THE INVENTION

001 This invention generally relates to microelectronic integrated circuit (IC) semiconductor device fabrication and more particularly to a method for forming a reduced active area of a phase change memory element to reduce a required phase changing electrical current.

BACKGROUND OF THE INVENTION

002 Phase change memory devices use phase changing materials, for example, materials where a phase change can be induced by an electrical energy, where a sufficient thermal heat induced by this electrical energy will result in a temperature change in the phase change materials, for example a current or voltage applied to the material to induce heating in the phase changing material. For example, the phase changing material may change between amorphous and crystalline including partially amorphous and partially crystalline, the nature of the phased state being

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detectable, for example by a number of order in resistance change, typically is larger than one order, and thereby forming stored information. Typical phase changing materials suitable for memory elements include those utilizing various chalcogenide elements, for example one or more elements from Column VI of the periodic table. One particularly suitable group of alloys is the GeSbTe alloys system.

003 Phase changing memory elements have several advantages over other types of memory including DRAM, SRAM, and Flash memory. For example, they are non-volatile and may be written to with high speed, e.g., less than about 50 nanoseconds. Since transistors are not necessary to accomplish the read and write operations, the memory cells may be formed at high density. In addition, such memory cells are compatible with CMOS logic and are low power and low cost.

004 One goal for producing phase changing memory cells is to reduce the power consumption by reducing the amount of drive current required to effect a phase change in the phase changing memory element. The required drive current is dictated by the resistance of the phase changing material as well as the active

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area of the phase changing material, which is dictated by the area to which electric contact is made to the phase changing material (phase change memory element) to deliver a phase changing current. In general, assuming a given resistance of the phase changing material, a smaller contact area produces a higher resistance and therefore a higher level of resistive heating (temperature) for a given applied writing (drive) current. Therefore a smaller electrode contact area to the phase changing material memory element will correspondingly and desirably reduce drive current and thereby power consumption.

005 There have been various approaches in the prior art to reduce the phase change memory cell electrode contact area (active area). In general, prior art approaches have relied on photolithographic and etching techniques to pattern and form as small a contact area as possible. These approaches are difficult to scale down in size due the limited processing windows in lithographic and etching processes at the desired sizes. Other approaches have relied on forming complicated memory cell structures that rely on complicated and therefore costly processing steps to produce various memory elements and

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electrode shapes.

006 Thus, there is a need in the semiconductor manufacturing art for an improved phase change memory element and method for forming the same to reduce an electrical contact area to the memory element thereby reducing power consumption.

007 It is therefore an object of the invention to provide an improved phase change memory element and method for forming the same to reduce an electrical contact area to the memory element thereby reducing power consumption, while overcoming other shortcomings and deficiencies of the prior art.

SUMMARY OF THE INVENTION

008 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a phase change memory structure and method for forming the same.

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009 In a first embodiment, the method includes a phase change memory structure and method for forming the same, the method including providing a substrate comprising a conductive area; forming a spacer having a partially exposed sidewall electrode at an upper portion of the spacer defining a phase change memory element contact area; and, wherein the spacer bottom portion partially overlaps the conductive area.

0010 These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention, which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

0011 Figures 1A-1F are cross sectional view of a portion of a phase change memory cell at manufacturing stages according to an embodiment of the present invention.

0012 Figures 2A and 2B are cross sectional views of a portion of a phase change memory cell according to embodiments of the present invention.

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0013 Figure 3 is a process flow diagram including several embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

0014 Although the phase change memory structure and method of forming the same is explained with reference to an exemplary memory cell, it will be appreciated that the spacer electrode and spacer memory elements formed according to embodiments of the invention may be used in the formation of other memory cell structures where a spacer is formed with exposed sidewall electrode at an upper portion to form a contact area of phase change memory element.

0015 Referring to Figure 1A, in one embodiment of the present invention a first inter-layer dielectric (ILD) 12 formed of a conventional silicon oxide dielectric such as PECVD silicon oxide is formed over a substrate (not shown) where the ILD layer includes a conductive area, for example a plug 14A formed by conventional damascene methods. The conductive plug may be

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formed of conductive materials such as W, TiN, TiW, TiAl, or TiAlN, or combinations thereof. It will be appreciated that the first ILD layer 12 may be formed of a variety of dielectric insulating materials including PECVD oxide, PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K ($K < 2.9$) dielectrics, and fluorine doped silicate glass (e.g., FSG). The conductive plug e.g., 14A provides electrical connection to a current driving circuit (not shown), for example including CMOS devices.

0016 Referring to Figure 1B, a dielectric layer portion 16 (mesa dielectric) formed of a dielectric insulating material such as silicon oxide, preferably PECVD oxide, deposited over the ILD layer 12 and lithographically patterned and etched to form the dielectric portion 16. It will be appreciated that the dielectric layer portion 16 may be formed of one or more of the same preferred insulating dielectrics as outlined for the first ILD layer. The dielectric portion 16 need not be, but in the present embodiment is shown formed overlapping a portion of the conductive plug 14A.

0017 Referring to Figure 1C, a conductive layer is first blanket deposited by conventional CVD or PVD methods over the

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process surface followed by etching back the conductive layer by a conventional dry and/or wet etching process to form conductive spacer 18A adjacent the dielectric portion 16 (sidewall) and partially overlapping the conductive plug 14A. Preferably the conductive spacer 18A is formed of a highly conductive material readily etchable such as W, TiN, TiW, TiAl, or TiAlN, or combination thereof. It will be appreciated that the maximum width of the spacer 18A may be formed with a variable maximum width dimension including adjusting the amount by which the spacer partially overlaps the conductive plug 14A, thus adjusting a resistance of the spacer (e.g., electrode).

0018 Referring to Figure 1D, in an important aspect of the invention, a conventional spin-on-layer (SOL) 20, formed of organic or inorganic material such a spin-on-glass, spin-on dielectric (SOD), benzocyclobutene, or polyimides (polyimides), is blanket deposited to cover the spacer 18A, followed by a wet and/or dry etchback process carried out for a predetermined period of time to uncover (expose) a predetermined portion of the top portion of spacer 18A, e.g., A, the exposed portion forming an electrode contact area (phase changing memory element electrode contact area) to a subsequently formed overlying upper

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electrode. For example, since the outer portion spacer is 18A is formed with an exposed sidewall electrode, etchback of the SOL may be carried for a predetermined time period to uncover a selected amount of the spacer 18A top portion, e.g., A, thus forming an adjustable electrode contact area. Thus, the phase changing memory element electrode contact area (electrode contact area) e.g., A, may be determined by the etching back process, for example an etching back time period. The electrode contacting area to the phase changing memory element is preferably as small as possible, typically is less than about 10000 nm², more preferably less than about 1000 nm², even more preferably less than about 100 nm².

0019 Referring to Figure 1E, a temperature sensitive (phase change triggering) phase changing (structure changing) material layer, for example a chalcogenide including Ge, Te, and Sb, is blanket deposited by a conventional deposition process followed by a photolithographic patterning of the phase changing layer and a wet and/or dry etching process to form a phase change memory element portion 22A in contact with the exposed upper portion (electrode contact area), e.g., A of the conductive spacer 18A bottom electrode. It will be appreciated that the

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dimensions of the memory element portion 22A may be varied, for example shown to be about the same width as the bottom electrode (conductive plug 14A) but may be formed having larger or smaller dimensions. Preferably, however, the memory element portion is formed at least large enough to cover the exposed portion of the bottom electrode, e.g., A which is determined by the etchback time to uncover a predetermined portion of the upper portion of the spacer 18A.

0020 Referring to Figure 1F, a second ILD layer 24A formed of the same preferred materials as the first ILD layer 12 is deposited and planarized, to electrically isolate the memory element portion 22A, followed by formation of a third planar ILD layer 24B over the second ILD layer followed by formation of a conductive plug e.g., 26A to form an upper electrode according to similar processes and preferred materials outlined for forming the first ILD layer 12 and conductive plug 14A.

0021 Referring to Figure 2A is shown an exemplary memory cell formed by the previously outline steps. For example conductive plugs 14A and 14B are formed in ILD layer 12, spacers 18A and 18B forming bottom electrodes, and an exposed bottom electrode

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contact area e.g., A, exposed for contacting a phase change memory elements e.g., 22A and 22B determined by etchback of SOL layer 20. Dielectric portion 16 is shown formed overlapping a portion of conductive plugs 14A and 14B allowing formation of thinner spacer bottom electrodes 18A and 18B. Phase change memory elements 22A and 22B are formed to encompass the electrode contact areas e.g., A to form a memory element contact areas over respective spacer bottom electrodes 18A and 18B. Second and third ILD layers 24A and 24B including conductive upper electrode portions 26A and 26B are then formed as previously outlined.

0022 Referring to Figure 2B, in another embodiment a similar series of process steps as outlined for Figures 1A through 1F are carried out to form a memory cell except that spacers 28A and 28B now form the phase changing material memory elements where an etchback process of SOL layer 20 exposes a portion e.g., B of the upper portion of the spacers to form a memory element electrode contact area with the top electrode. In this embodiment, the dielectric portion 16 is not formed to partially overlap the conductive plugs 14A and 142B, which now form the bottom electrodes. In this embodiment the bottom electrode

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contact area may be adjusted by determining the overlap width, W1, the spacers 28A and 28B overlap the conductive plugs 14A and 14B.

0023 Still referring to Figure 2B, upper electrode portions 30A and 30B are preferably formed of the same preferred conductive materials as the conductive plugs 14A and 14B, and may be formed of the same or different preferred materials. For example, a deposition, lithographic and wet or dry etchback process is carried out to form the upper electrodes 30A and 30B. In this embodiment, only a second ILD layer 24A is required to electrically isolate the upper electrodes 30A and 30B. Similar to the first embodiment the memory element electrode contact area (active area) is formed having an area less than about 10000 nm^2 , more preferably less than about 1000 nm^2 , even more preferably less than about 100 nm^2 .

0024 Thus, a phase change memory structure and method for forming the same to selectively form an active area to reduce a required drive current has been presented. Advantageously, spacer elements having an exposed sidewall in an upper portion may be formed and an etchback process may be carried out to

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uncover a selected portion of the upper portion of the spacer element to form a memory element electrode contact area (active area). In one embodiment the spacer elements 28A and 28B are formed of a phase change material overlapping on the bottom electrode 14A and 14B. In another embodiment, the spacer elements are formed of a phase changing material where the uncovered upper portion forms an upper electrode contact area. Advantageously, the process steps may be carried out easily and cost effectively, being compatible with existing CMOS formation processes. Advantageously, the memory element electrode contact area (active area), producing a programmable memory volume of the phase change memory element, may be adjustably formed, for example, reduced to decrease a programmable drive current thereby lowering power consumption.

0025 Referring to Figure 3 is a process flow diagram including several embodiments of the present invention. In process 301, an ILD layer including a conductive plug is provided. In process 303, a mesa top dielectric portion is formed over the ILD layer. In process 305, spacer elements forming one of a memory element and memory electrode are formed adjacent the mesa top dielectric portion to overlap a portion of the conductive plug. In process

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307, the spacer are covered by an SOL layer an upper portion uncovered to form a phase change memory element contact area. In process 309, the memory cell is completed including forming either a memory element over a respective bottom electrode spacer or an upper electrode over a respective spacer memory element.

0026 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.